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Kind regards,

Team Nexperia

DATA SHEET

74F109

Positive J- $\bar{K}$ positive edge-triggered
flip-flops

Product specification

1990 Oct 23

IC15 Data Handbook

Postive J-K positive edge-triggered flip-flops

74F109

FEATURE

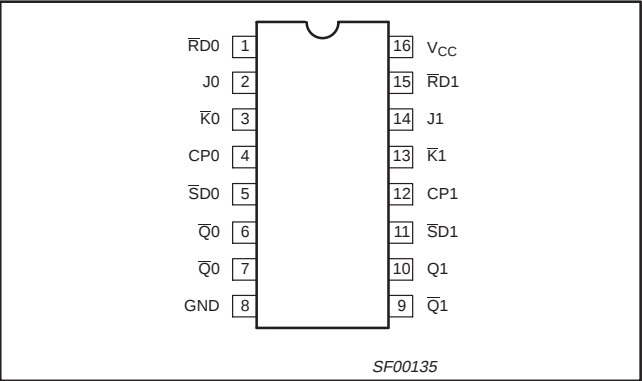
- Industrial temperature range available (−40°C to +85°C)

DESCRIPTION

The 74F109 is a dual positive edge-triggered JK-type flip-flop featuring individual J, K, clock, set, and reset inputs; also true and complementary outputs. Set ($\overline{SD}$) and reset ($\overline{RD}$) are asynchronous active low inputs and operate independently of the clock (CP) input. The J and K are edge-triggered inputs which control the state changes of the flip-flops as described in the function table. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. The J and $\overline{K}$ inputs must be stable just one setup time prior to the low-to-high transition of the clock for predictable operation. The JK design allows operation as a D flip-flop by tying J and $\overline{K}$ inputs together. Although the clock input is level sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock to output delay time for reliable operation.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F109	125MHz	12.3mA

PIN CONFIGURATION



ORDERING INFORMATION

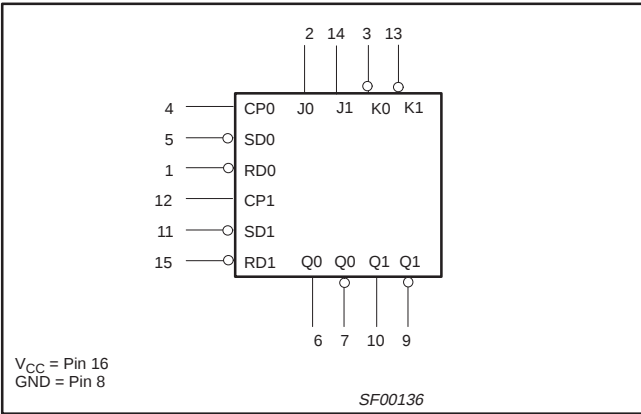
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$	
16-pin plastic DIP	N74F109N	I74F109N	SOT38-4
16-pin plastic SO	N74F109D	I74F109D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

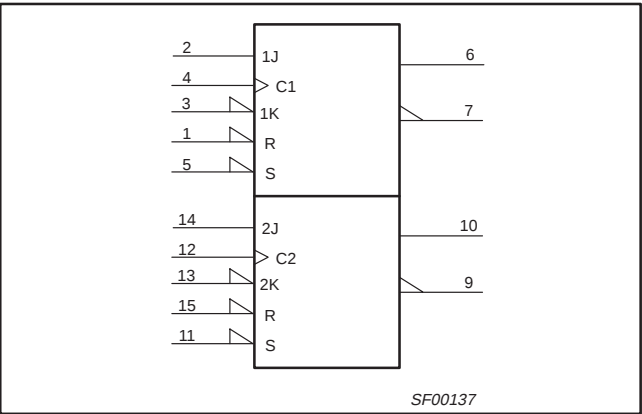
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J0, J1	J inputs	1.0/1.0	20 μ A/0.6mA
K0, K1	K inputs	1.0/1.0	20 μ A/0.6mA
CP0, CP1	Clock inputs (active rising edge)	1.0/1.0	20 μ A/0.6mA
$\overline{SD}$ 0, $\overline{SD}$ 1	Set inputs (active Low)	1.0/3.0	20 μ A/1.8mA
$\overline{RD}$ 0, $\overline{RD}$ 1	Reset inputs (active Low)	1.0/3.0	20 μ A/1.8mA
Q0, Q1, $\overline{Q}$ 0, $\overline{Q}$ 1	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



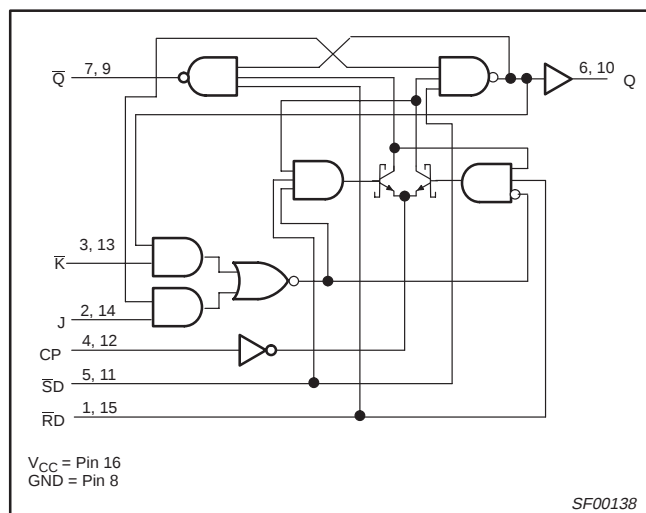
IEC/IEEE SYMBOL



Positive J- $\bar{K}$ positive edge-triggered flip-flops

74F109

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\bar{S}D$	$\bar{R}D$	CP	J	$\bar{K}$	Q	$\bar{Q}$	
L	H	X	X	X	H	L	Asynchronous set
H	L	X	X	X	L	H	Asynchronous reset
L	L	X	X	X	H	H	Undetermined*
H	H	$\uparrow$	X	X	q	$\bar{q}$	Hold
H	H	$\uparrow$	h	l	$\bar{q}$	q	Toggle
H	H	$\uparrow$	h	h	H	L	Load "1" (set)
H	H	$\uparrow$	l	l	L	H	Load "0" (reset)
H	H	$\uparrow$	l	h	q	$\bar{q}$	Hold 'no change'

NOTES:

H = High-voltage level

h = High-voltage level one setup time prior to low-to-high clock transition

L = Low-voltage level

l = Low-voltage level one setup time prior to low-to-high clock transition

q = Lower case indicate the state of the referenced output prior to the low-to-high clock transition

X = Don't care

 $\uparrow$ = Low-to-high clock transition $\uparrow$ = Not low-to-high clock transition* = Both outputs will be high if both $\bar{S}D$ and $\bar{R}D$ go low simultaneously

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T_{stg}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IN}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	Commercial range	0	+70	°C
		Industrial range	-40	+85	°C

Postive J-K̄ positive edge-triggered flip-flops

74F109

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			MIN	TYP ²	MAX	
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = MAX	±10%V _{CC}	2.5	V
				±5%V _{CC}	2.7	V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = MAX	±10%V _{CC}	0.30	V
				±5%V _{CC}	0.30	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-0.73	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			100	μA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA
I _{IL}	Low-level input current	J, K̄, CPn	V _{CC} = MAX, V _I = 0.5V		-0.6	mA
		SDn, RDn	V _{CC} = MAX, V _I = 0.5V		-1.8	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		-60	-150	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX		12.3	17	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Measure I_{CC} with the clock input grounded and all outputs open, then with Q and Q̄ outputs high in turn.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS								UNIT
			V _{CC} = +5.0V T _{amb} = +25°C C _L = 50pF R _L = 500Ω			V _{CC} = +5.0V ± 10% T _{amb} = 0°C to +70°C C _L = 50pF R _L = 500Ω		V _{CC} = +5.0V ± 10% T _{amb} = −40°C to +85°C C _L = 50pF R _L = 500Ω			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f _{MAX}	Maximum clock frequency	Waveform 1	90	125		90		90		MHz	
t _{PLH} t _{PHL}	Propagation delay CPn to Qn or Q̄n	Waveform 1	3.8 4.4	5.3 6.2	7.0 8.0	3.8 4.4	8.0 9.2	3.8 4.4	9.0 9.2	ns	
t _{PLH} t _{PHL}	Propagation delay SDn, RD to Qn or Q̄n	Waveform 2, 3	3.2 3.5	5.2 7.0	7.0 9.0	3.2 3.5	8.0 10.5	2.8 3.5	9.0 10.5	ns	

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS								UNIT
			V _{CC} = +5.0V T _{amb} = +25°C C _L = 50pF R _L = 500Ω			V _{CC} = +5.0V ± 10% T _{amb} = 0°C to +70°C C _L = 50pF R _L = 500Ω		V _{CC} = +5.0V ± 10% T _{amb} = −40°C to +85°C C _L = 50pF R _L = 500Ω			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{su} (H) t _{su} (L)	Setup time, high or low Dn to CPn	Waveform 1	3.0 3.0			3.0 3.0		3.0 3.0		ns	
t _h (H) t _h (L)	Hold time, high or low Dn to CPn	Waveform 1	1.0 1.0			1.0 1.0		1.0 1.0		ns	
t _w (H) t _w (L)	CP pulse width, high or low	Waveform 1	4.0 5.0			4.0 5.0		4.0 5.0		ns	
t _w (L)	$\overline{\text{SDn}}$ or $\overline{\text{RDn}}$ pulse width, low	Waveform 2	4.0			4.0		4.0		ns	
t _{rec}	Recovery time $\overline{\text{SDn}}$ or $\overline{\text{RDn}}$ to CP	Waveform 3	2.0			2.0		2.0		ns	

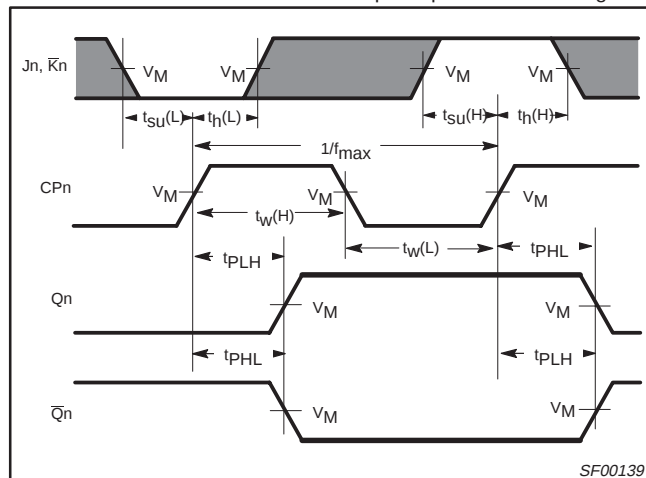
Postive J- $\bar{K}$ positive edge-triggered flip-flops

74F109

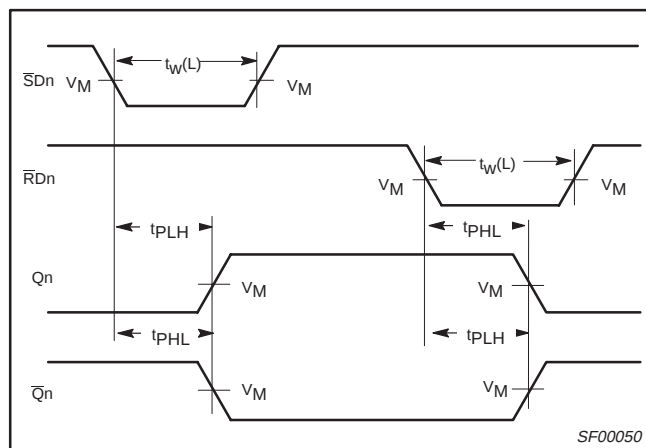
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.

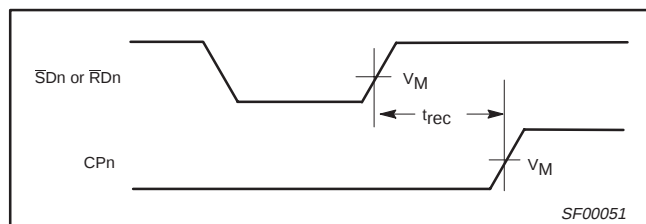
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times, and Clock Width, and Maximum Clock Frequency



Waveform 2. Propagation Delay for Set and Reset to Output, Set and Reset Pulse Width

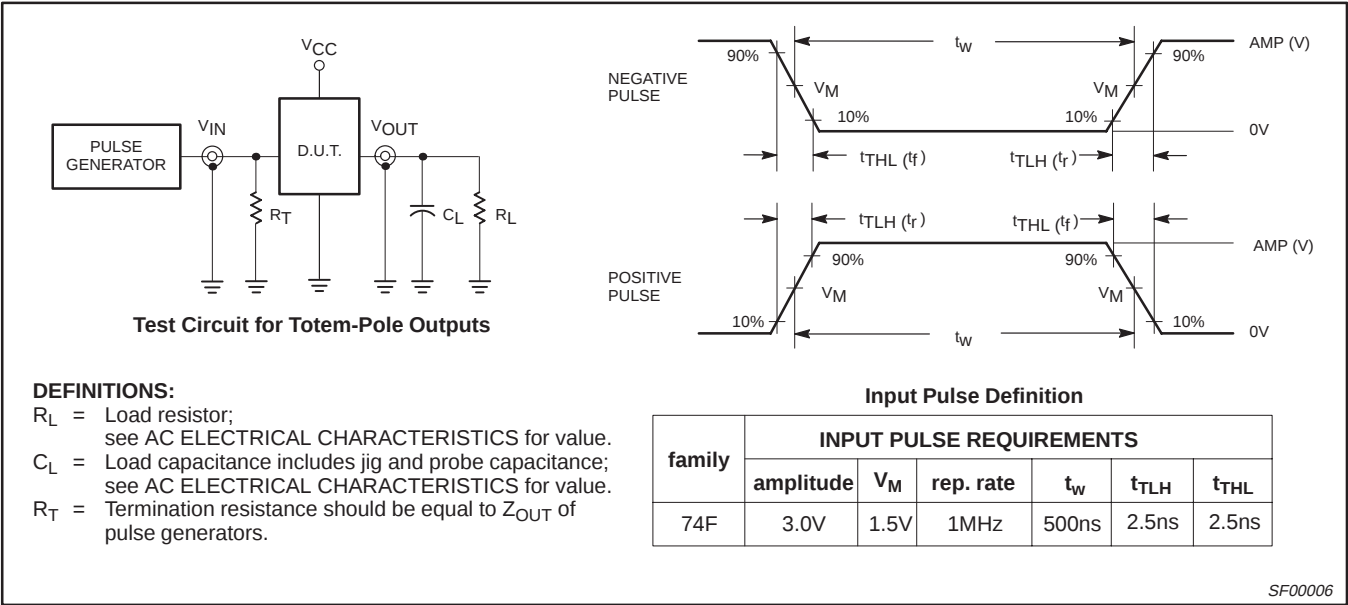


Waveform 3. Recovery Timer for Set or Reset to Clock

Postive J-K positive edge-triggered flip-flops

74F109

TEST CIRCUIT AND WAVEFORMS

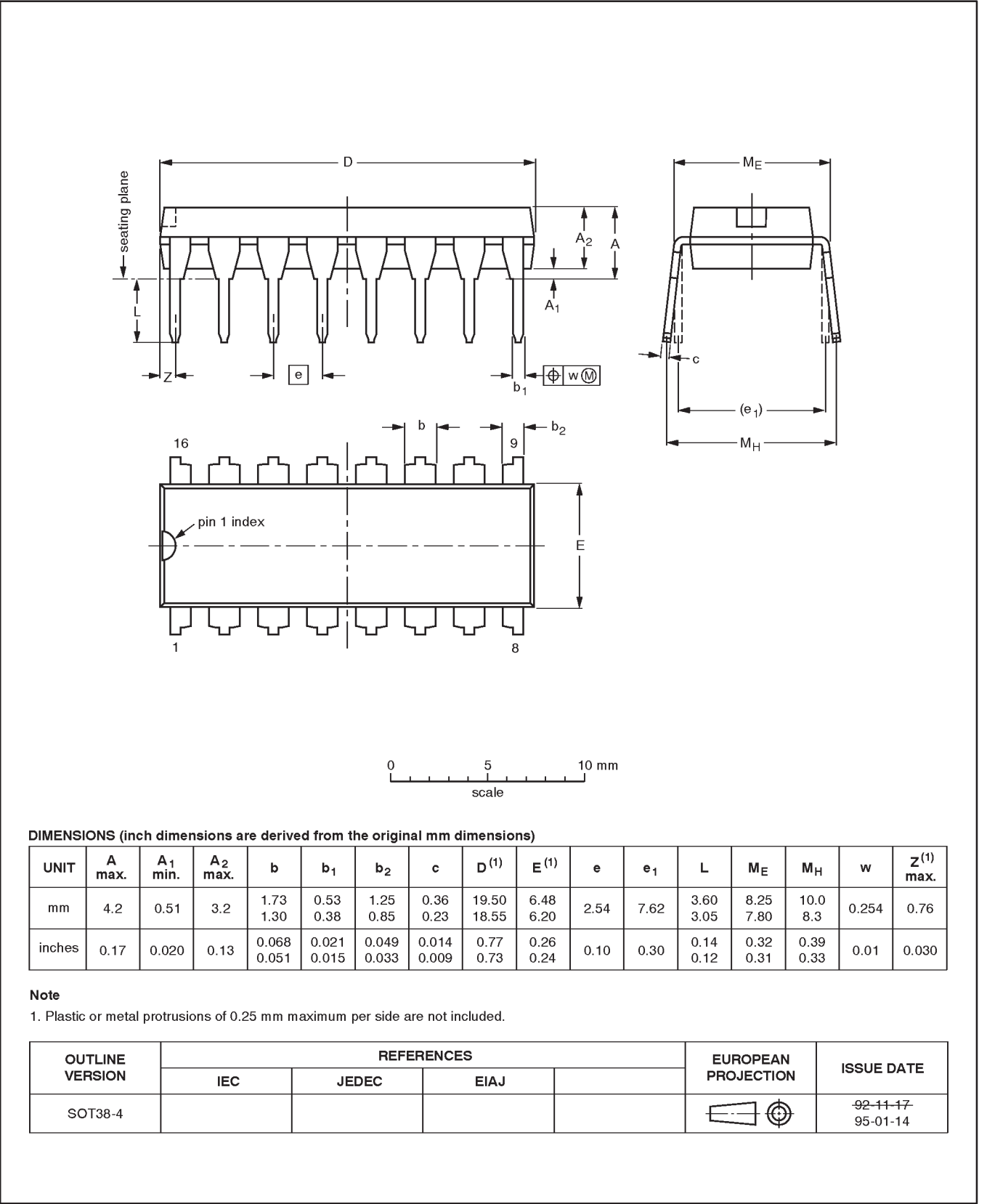


Positive J-K positive edge-triggered flip-flops

74F109

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

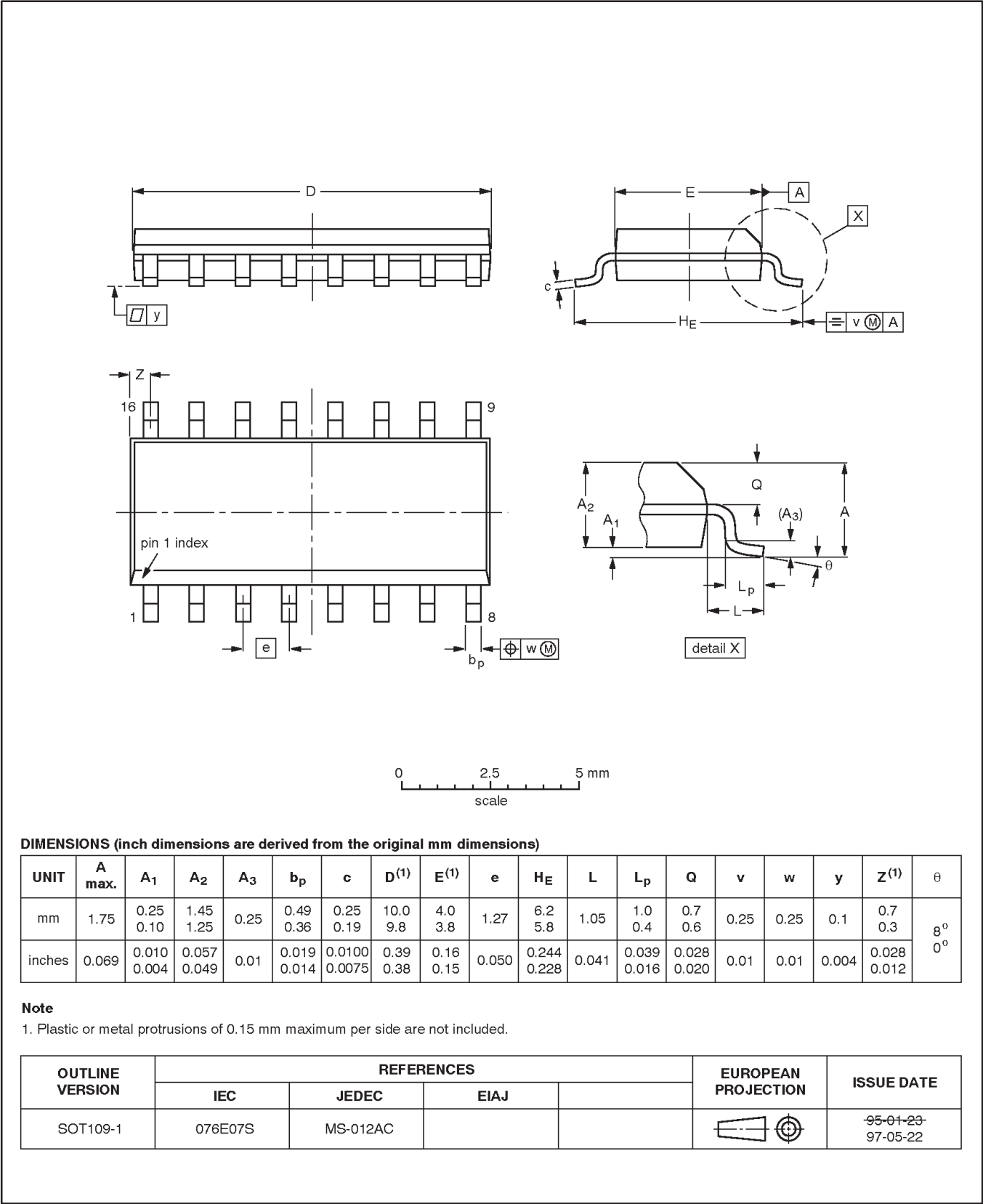


Positive J-K positive edge-triggered flip-flops

74F109

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Positive J- $\bar{K}$ positive edge-triggered flip-flops

74F109

NOTES

Positive J-K positive edge-triggered flip-flops

74F109

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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